Claims

What is claimed is:

[c1] A flip-flop circuit with embedded scan capabilities and having a master stage and a slave stage, comprising:

a data input control stage that selectively controls a value on a data node that is coupled to the master stage and the slave stage; and

a scan input control stage that selectively controls a value on a scan node that is coupled to the master stage.

[c2] The flip-flop circuit of claim 1, wherein the data input control stage inputs a data input signal and a scan enable signal, and wherein the data input control stage resides on one end of the flip-flop circuit.

[c3] The flip-flop circuit of claim 1, wherein the scan input control stage inputs a scan input signal and a scan enable signal, and wherein the scan input control stage resides on another end of the flip-flop circuit.

[c4] The flip-flop circuit of claim 1, the master stage comprising:

a skewed latch that pulls the data node to a first value when the flip-flop circuit is in a scan mode.

[c5] The flip-flop circuit of claim 4, wherein the scan node is active during the scan mode.

[c6] The flip-flop circuit of claim 4, wherein the skewed latch pulls the scan node to a second value when the flip-flop circuit is in a normal mode, and wherein the data node is active during the normal mode.

[c7] The flip-flop circuit of claim 1, wherein the master stage passes a value to the

slave stage based on the values of the scan node and the data node.

[c8] The flip-flop circuit of claim 1, further comprising:

a clock input control stage that generates delayed and inverted clock signals to the data input control stage, the scan input control stage, the master stage, and the slave stage.

[c9] The flip-flop circuit of claim 8, wherein a data input signal selectively controls the value on the data node dependent upon the clock input control stage.

[c10] The flip-flop circuit of claim 8, wherein a scan input signal selectively controls the value on the scan node dependent upon the clock input control stage.

[c11] The flip-flop circuit of claim 8, wherein the master stage selectively passes a value to the slave stage dependent upon the data node, the scan node, and the clock input control stage.

[c12] The flip-flop circuit of claim 8, wherein the slave stage selectively controls an output of the flip-flop circuit dependent upon the data node and the clock input control stage.

[c13] A method for performing operations using a flip-flop with embedded scan capabilities and having a master stage and a slave stage, comprising:

selectively controlling a value on a data node dependent upon a data input control stage and a clock input control stage, wherein the data node is coupled to the master stage and the slave stage;

selectively controlling a value on a scan node dependent upon a scan input control stage and the clock input control stage, wherein the scan node is coupled to the master stage;

selectively controlling the slave stage dependent upon the master stage and the clock input control stage; and

selectively generating an output of the flip-flop dependent upon the slave stage.

[c14] The method of claim 13, further comprising:

selectively holding the data node to a first value when the flip-flop is in a scan mode.

[c15] The method of claim 14, wherein the scan node is active during the scan mode.

[c16] The method of claim 13, further comprising:

selectively holding the scan node to a second value when the flip-flop is in a normal mode.

[c17] The method of claim 16, wherein the data node is active during the normal mode.

[c18] The method of claim 13, further comprising:

inputting a clock signal to the clock input control stage; and

selectively generating delayed and inverted versions of the clock signal therefrom.